AMENDMENTS TO THE SPECIFICATION:

Please REPLACE the paragraph bridging pages 1 and 2 of the Specification with the following amended paragraph:

The MIM capacitor is constructed such that the silicon nitride layer is positioned between silicon oxide layers in order to complement the withstand voltage of the silicon nitride layer. The MIM capacitor however has a problem that the overall dielectric constant becomes lower because silicon oxide has a dielectric constant lower than that of silicon nitride. Also, when the MIM capacitor is prepared on the Ga-As substrate at 400° C or more, As is liberated and thus the Ga-As substrate deteriorates. Further, when the silicon oxide layers and the silicon nitride layer are deposited at 400° C by a ~~CVC~~ CVD method, thin and flat silicon oxide layers cannot be formed with half or less than half the thickness of the silicon nitride layer. Hence, a dielectric layer of the MIM capacitor composed of three layers, which are the silicon oxide layer, the silicon nitride layer, and the silicon oxide layer, has twice or more than twice the thickness of a dielectric layer simply composed of silicon nitride layers. Thus, preparing a high-capacity bypass capacitor with an MIM capacitor makes preparing small MMICs difficult because of the large MIM capacitor.